foregoing heat treatment, by forming the p^+ layer by the vapor growth technique after forming the n^+ embedded layer **23** by the diffusion technique, by the use of the direct wafer joining technique, etc.

Further, in the fifth embodiment wherein the n^+ embedded layer **23** is formed in the p^+ layer **11**, the pattern of the n^+ embedded layer **23** may be modified, as in the foregoing second, third and fourth embodiments, if the object of the n^+ embedded layer **23** is accomplished.

In all the embodiments, the high-voltage withstand region **3** is not necessarily formed depending on the service condition of the IGBT.

Although all the embodiments use the p type and n type as the first conduction type and second conduction type, respectively, the present invention is valid even when the opposite conduction type is used.

INDUSTRIAL APPLICABILITY

As described above, the insulated gate bipolar transistor according to the present invention is usable as a power element for which high withstand voltage and low on-resistance are required, and when used as a power switching element of power converting units such as inverters for driving motors in PWM (pulse width modulation) control mode, it is very effective because its built-in reverse conducting function can circulate the motor current.

What is claimed is:

1. An insulated gate bipolar transistor with a reverse conducting function comprising:

a first semiconductor layer of a first conduction type;

a second semiconductor layer of a second conduction type formed in contact with the first semiconductor layer at a bottom surface therebetween;

a third semiconductor region of the first conduction type formed in the second semiconductor layer and having a junction portion extending to a top surface of said second semiconductor layer;

a fourth semiconductor region of the second conduction type formed in the third semiconductor region and having a junction portion extending to said top surface of said second semiconductor layer;

an insulated gate electrode formed at least over the third semiconductor region junction portion laterally extending between the fourth semiconductor region junction portion and a non-diffused potion of said second semiconductor layer which extends to the top surface thereof;

a source electrode in contact with both the third semiconductor region and the fourth semiconductor region;

a drain electrode for supplying a drain current through the first semiconductor layer;

a fifth semiconductor region of the second conduction type which is electrically connected to the drain electrode via an external conductor, and formed within the second semiconductor layer having a junction portion extending to said top surface of the second semiconductor layer so as to pass therethrough a reverse conducting current opposite in direction to the drain current;

a sixth semiconductor region of the second conduction type formed partially at or near the bottom surface between the first semiconductor layer and the second semiconductor layer, said sixth semiconductor region having an impurity concentration higher than that of the second semiconductor layer and formed into a given pattern to reduce an electric resistance on carriers passing between the fifth semiconductor region and a portion of the second semiconductor layer at a distance from the fifth semiconductor region, said sixth semiconductor region allowing the carriers to pass across the bottom surface between the first semiconductor layer and the second semiconductor layer; and

an electrically isolated high-voltage withstand region provided between said fifth semiconductor region and an element region, said element region including at least said second semiconductor layer, said third semiconductor region and said fourth semiconductor region, said high-voltage withstand region providing a high voltage withstand barrier against high voltages produced in an end area of said element region,

said sixth semiconductor region being provided below at least said element region and said high-voltage withstand region, and said given pattern of said sixth semiconductor region being such that at least a part of said sixth semiconductor region extends continuously from a portion below said element region to a portion below said high-voltage withstand region.

2. An insulated gate bipolar transistor according to claim **1**, wherein the sixth semiconductor region pattern provides contact portions and non-contact portions between the first and second semiconductor layers, said non-contact portions for passing the carriers therethrough when said transistor is active.

3. An insulated gate bipolar transistor according to claim **2**, wherein the sixth semiconductor region pattern is a mesh pattern or a striped pattern and is formed at least relative to a region confronting the third semiconductor region.

4. An insulated gate bipolar transistor according to claim **1**, wherein the sixth semiconductor region pattern is formed entirely in the first semiconductor layer at a close distance from the bottom surface of the second semiconductor layer, the distance being smaller than a diffusion length of minority carriers in the first semiconductor layer such that majority carriers pass between the first and second semiconductor layers.

5. An insulated gate bipolar transistor according to claim **4**, wherein the sixth semiconductor region pattern is a mesh pattern or a striped pattern and is formed at least relative to a region confronting the third semiconductor region.

6. An insulated gate bipolar transistor according to claim **1**, wherein the sixth semiconductor region pattern is a mesh pattern or a striped pattern and is formed at least relative to a region confronting the third semiconductor region.

7. An insulated gate bipolar transistor according to claim **6**, wherein the fifth semiconductor region is formed along a peripheral surface portion of the second semiconductor layer.

8. An insulated gate bipolar transistor according to claim **7**, wherein the sixth semiconductor region pattern is formed so as to spread up to a region confronting the fifth semiconductor region formed along the peripheral surface portion of the second semiconductor layer.

9. An insulated gate bipolar transistor according to claim **7**, wherein the sixth semiconductor region pattern is p^+ layer **11** (where the n layer **23** is present) as to formed so as to spread up to a region confronting both the fifth semiconductor region and the high-voltage withstand region.

10. An insulated gate bipolar transistor according to claim **9**, wherein said high-voltage withstand region includes a guard ring.

11. An insulated gate bipolar transistor according to claim **1**, wherein the fifth semiconductor region is formed along a